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APPLICATION FOR LETTERS PATENT

for

**WAFER-LEVEL CHIP SCALE PACKAGE AND METHOD FOR FABRICATING  
AND USING THE SAME**

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**WAFER-LEVEL CHIP SCALE PACKAGE AND METHOD FOR FABRICATING  
AND USING THE SAME**

[001]                    CROSS-REFERENCE TO RELATED APPLICATION

[002]                    This application is a continuation-in-part of U.S. Patent Application Number 10/618,113, which is a continuation-in-part of U.S. Patent Application No. 10/295,281, the entire disclosures of which are incorporated herein by reference.

[003]                    FIELD OF THE INVENTION

[004]                    The invention generally relates to methods for fabricating integrated circuits (ICs) and semiconductor devices and the resulting structures. Specifically, the invention relates to semiconductor packages and methods for fabricating and using such packages. More particularly, the invention relates to wafer level chip scale packages and methods for fabricating and methods for using such packages.

[005]                    BACKGROUND OF THE INVENTION

[006]                    Recent advancements in the electronics industry, especially with personal computers (PC), mobile phones, and personal data assistants (PDA), have triggered a need for light, compact, and multi-functional power systems that can process large amounts of data quickly. These advancements have also triggered a reduction in the size of semiconductor chips and the packaging used for these chips.

[007]                    The semiconductor chips typically have conductive pads formed at the top surface of the silicon substrate containing the IC. Wire bonding is used to connect the conductive pads on the substrate to corresponding pads on a package substrate. The increasing complexity of the circuitry in the IC has required the conductive pads to be formed closer together. With the bond pads narrower, the length of the wire (in the wire bonding) needs to be longer and width narrower which unfortunately induces a greater amount of inductance and thereby reduces the speed of the circuitry.

[008]                    One type of packaging that has been recently used is wafer-level chip size

packaging (WLCSP). See, for example, U.S. Patent Nos. 6187615 and 6287893, the disclosures of which are incorporated herein by reference.

[009] In general, to fabricate WLCSP, a wafer is processed and then packaged by a photolithography process and a sputtering process. This method is easier than general packaging processes that use die bonding, wire bonding, and molding. Processes for WLCSP also have other advantages when compared to general packaging processes. First, it is possible to make solder bumps for all chips formed on a wafer at a single time. Second, a wafer-level test on the operation of each semiconductor chip is possible during WLCSP processes. For these—and other reasons—WLCSP can be fabricated at a lower cost than general packaging.

[0010] Figures 1-3 illustrate several known wafer-level chip scale packages. As shown in FIG. 1, chip pads 40 are formed of a metal such as aluminum on a silicon substrate 5. A passivation layer 10 is formed to expose a portion of each of the chip pads 40 on the silicon substrate 5 while protecting the remainder of the silicon substrate 5. A first insulating layer 15 is formed over the passivation layer 10 and then a re-distribution line (RDL) pattern 20 (which re-distributes electrical signals from the bond pad 40 to solder bump 35) is formed over portions of the first insulating layer 15 and the exposed chip pads 40. A second insulating layer 25 is formed on portions of the RDL pattern 20 while leaving portions of the RDL pattern 20 exposed. Under bump metals (UBM) 30 are formed between solder bumps 35 and the exposed portions of the RDL pattern 20. The RDL pattern 20 contains inclined portions on the first insulating layer 15 near the chip pads 40. In these areas, short circuits can occur and the pattern 20 can crack and deform in these areas due to stresses.

[0011] As depicted in FIG. 2, package 50 contains an RDL pattern 54 that adheres to a solder connection 52 in a cylindrical band. Such a configuration has several disadvantages. First, the contact area between the RDL pattern 54 and the solder connection 52 is minimal, thereby deteriorating the electrical characteristics between them. Second, short circuits may occur due to the stresses in the contact surface between the RDL pattern 54 and the solder connection 52. Third, the solder connection 52—

which is connected with a solder bump 58 formed on a chip pad 56—is exposed to the outside of the package 50, i.e., to air. Thus, there is a higher possibility that moisture penetrates into the solder connection 52 and decreases the reliability of the solder connection 52. Fourth, the package 50 is completed only by carrying out many processing steps and, therefore, manufacturing costs are high.

[0012] As shown in FIG. 3, package 60 contains a RDL pattern 76 that is electrically connected with a chip pad 72 via a connection bump 74. The RDL pattern 76 is, however, inclined on the connection bump 74, causing cracks therein due to stresses as described above. As well, the connection bump 74 is made by a plating process and is formed of aluminum, copper, silver, or an alloy thereof. Accordingly, the package 60 is not easy to manufacture.

[0013] Other problems exist with conventional WLSCP. Often, such packaging uses UMB (i.e., layer 30 in FIG. 1) and two insulating layers (i.e., layers 15 and 25 in FIG.1) that are made of polymeric materials such as polyimide and benzocyclobutene (BSB). Such structures are complicated to manufacture. As well, the coefficient of thermal expansion (CTE) between the various layers can induce thermal stresses into the ICs and damage the ICs during high temperature curing of these polymeric materials.

[0014] As well, conventional packaging methods have used a conductive film or paste in flip chip packaging. See, for example, U.S. Patent No. 6,509,634, the disclosure of which is incorporated herein by reference. Generally, these methods used a gold bump on a silicon die and then bonded it to a substrate (usually ceramic) using the conductive film or paste using ultrasonic bonding. Such methods, however, suffer from a high cost and poor reliability.

[0015] SUMMARY OF THE INVENTION

[0016] The invention provides a packaged semiconductor device (a wafer-level chip scale package) containing an adhesive film containing conductive particles sandwiched between a chip with Cu-based stud bumps and a substrate containing a bond pad. Some

conductive particles are sandwiched between the stud bump and bond pad to create a conductive path. The wafer level chip scale package is manufactured without the steps of dispensing solder and reflowing the solder and can optionally eliminate the use of a redistribution trace. Using such a configuration increases the reliability of the wafer-level chip scale package

[0017]                                    BRIEF DESCRIPTION OF THE DRAWINGS

[0018]                    Figures 1-30 are views of one aspect of the devices and methods of making the devices according to the invention, in which:

[0019]                    Figure 1 is a cross-sectional view of a conventional wafer-level chip scale page;

[0020]                    Figure 2 is a cross-sectional view of another conventional wafer-level chip scale package;

[0021]                    Figure 3 is a cross-sectional view of another conventional wafer-level chip scale package;

[0022]                    Figure 4 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0023]                    Figure 5 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0024]                    Figure 6 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0025]                    Figure 7 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0026]                    Figure 8 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0027]                    Figure 9 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0028]                    Figure 10 is a cross-sectional view showing a stage in a method of fabricating a wafer-level chip scale package according to an aspect of the invention;

[0029]                    Figure 11 is a cross-sectional view of a wafer-level chip scale package according

to one aspect of the invention;

[0030] Figures 12-15 illustrate stages in a method of fabricating a wafer-level chip scale package in one aspect of the invention;

[0031] Figure 16 depicts another stage in a method of fabricating a wafer-level chip scale package in one aspect of the invention;

[0032] Figure 17 depicts a process for making a wafer-level chip scale package in another aspect of the invention;

[0033] Figures 18-25 illustrate stages in a method of fabricating a wafer-level chip scale package in one aspect of the invention;

[0034] Figure 26 depicts conductive particles that can be used in one aspect of the invention;

[0035] Figures 27 depicts a wafer-level chip scale package in one aspect of the invention;

[0036] Figure 28 shows stages in a method of fabricating a wafer-level chip scale package in one aspect of the invention; and

[0037] Figures 29-30 illustrate stages in a method of fabricating a wafer-level chip scale package in one aspect of the invention

[0038] Figures 1-30 presented in conjunction with this description are views of only particular—rather than complete—portions of the devices and methods of making the devices according to the invention. Together with the following description, the Figures demonstrate and explain the principles of the invention. In the Figures, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being “on” another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. The same reference numerals in different drawings represent the same element, and thus their descriptions will be omitted.

[0039] DETAILED DESCRIPTION OF THE INVENTION

[0040] The invention now will be described more fully with reference to the accompanying drawings, in which one aspect of the invention is shown. This invention may, however, be embodied in many different forms and should not be construed as being

limited to the aspects set forth herein. Rather, these aspects are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art. Although the invention is described with respect to IC chips, the invention could be used for other devices where packaging is needed, i.e., silicon MEMS devices, LCD displays, optoelectronics, and the like.

[0041] FIGS. 4 through 10 illustrate one aspect of the invention for fabricating a wafer-level chip scale package containing a re-distributed line (RDL) pattern that is not inclined between the bottom of a solder bump and the top surface of a chip pad. Referring to FIG. 4, a substrate (or chip) 100 is prepared on which a passivation layer 110 and a chip pad 115 are formed. The substrate 100 can be any known semiconductor substrate known in the art, including "compound" semiconductors and single crystal silicon. The passivation layer 110 can be made of any dielectric material known in the art, such as silicon nitride, silicon oxide, or SOG.

[0042] Then, the chip pad 115 is formed on the upper surface of substrate 100. First, a portion of passivation layer in this area is removed by a conventional masking and etching process. Then, the metal for the chip pad 115 is blanket deposited and the portions of the metal layer not needed for the bond pad are removed by etching or planarization. The chip pad 115 can be made of conductive material, such as metals and metal alloys. In one aspect of the invention, the chip pad comprises aluminum.

[0043] A wire 120 is next attached to the chip pad 115 using a capillary 130. As shown in FIG. 5, the bottom of the wire 120 is bonded to the chip pad 115. Then a coining process is performed to press the wire 120 under a predetermined pressure, thereby forming a coined stud bump 125. By using the capillary 130, the coined stud bump 125 can be formed with a simple structure and with a simple manufacturing process.

[0044] As depicted in FIG. 6, a first insulating layer 135 is then deposited to cover the coined stud bump 125 and passivation layer 110. In this aspect of the invention, the first insulating layer 135 is formed of a dielectric polymer material such as BCB, polyimide (PI), and epoxy molding compound (EMC). As illustrated in FIG. 7, the first insulating layer 135 and the coined stud bump 125 are planarized using conventional processing. In

the planarization process, a stud bump 125' and a first insulating layer 135' as formed. In one aspect of the invention, a chemical mechanical polishing (CMP) process is used to planarize the first insulating layer 135 and the stud bump 125.

[0045] As shown in FIG. 8, a re-distributed line (RDL) pattern 140 is formed on the stud bump 125' and the first insulating layer 135'. The RDL pattern 140 electrically connects the stud bump 125' and the solder bump that is formed during subsequent processing (as described below). The RDL pattern is formed by blanket depositing a metal layer and then removing—typically by masking and etching—the portions of the metal layer not needed for the RDL pattern 140. The RDL pattern 140 can contain any electrically conductive material, such as metals and metal alloys. Examples of such metal and metal alloys include Cu, Al, Cr, NiV, and Ti. In one aspect of the invention, the RDL comprises a composite layer of Cu, Al, Cr, and Cu, or a material selected from NiV and Ti. In conventional wafer-level chip scale package as shown in FIG. 1, the RDL pattern 20 was formed of Al, NiV, Cu, NiV, and Cu that are sequentially deposited on the chip pad 40. Such a configuration has poor adhesive characteristics and reliability, is not easy to fabricate, and high manufacturing costs.

[0046] As depicted in FIG. 9, a second insulating layer 150 is then formed to cover the RDL pattern 140 and the first insulating layer 135'. A portion of the second insulating layer 150 is removed—typically by masking and etching—to expose a portion of the RDL pattern 140 to which a solder bump is later attached. As shown in FIG. 10, a solder bump 160 is then attached to the exposed portion of the RDL pattern 140 as known in the art. The stud bump comprises any conductive material such as metal and metal alloys. In one aspect of the invention, the stud bump comprises gold (Au) or copper (Cu).

[0047] The wafer-level chip scale package 1000 is illustrated in FIG. 10. The silicon substrate 100 contains an IC (not shown) and chip pad 115 which extends into the passivation layer 110 and is encircled by the passivation layer 110. Electrical signals from the IC contained in substrate 100 are transmitted through chip pad 115, through RDL pattern 140, to solder bump 160, and then to the outside of the packaged semiconductor device (i.e., to a circuit board).



[0048] In the device of FIG. 10, the first insulating layer 135' encircles and covers the stud bump 125'. Since the top surface of the first insulating layer 135' and stud bump 125' are coplanar in this aspect of the invention, the RDL pattern 140 may be formed as a substantially planar layer without an inclined portion. Therefore, cracks in the RDL pattern 140 due to stresses are prevented.

[0049] The RDL pattern 140 shown in FIG. 10 is illustrated as on only a portion of the upper surface of the stud bump 125'. In another aspect of the invention, the RDL pattern can be formed to cover the entire stud bump 125', thus enhancing the electrical characteristics and reliability of the wafer-level chip scale package 1000.

[0050] The RDL pattern 20 of FIG. 1 contains an inclined portion in the conventional wafer-level chip scale package. Accordingly, it is extremely difficult to form a thick first insulating layer 15 in FIG. 1. In this aspect of the invention, however, the first insulating layer 135' in FIG. 10 is formed as thick layer.

[0051] FIG. 11 illustrates another aspect of the invention where a wafer-level chip scale package has a two-layer RDL pattern. A wafer-level chip scale package 2000 contains: a substrate (or chip) 100; a passivation layer 110; chip pads 115; stud bumps 125' that are formed on chip pads 115 and are encircled by a first insulating layer 135'; intermediate RDL pattern 210 that connects the stud bumps 125' and intermediate stud bumps 220; an intermediate insulating layer 230 that insulates the intermediate RDL pattern 210; RDL pattern 140 that connects the intermediate stud bumps 220 and solder bumps 160; a second insulating layer 150 that insulates the RDL patterns 140; and solder bumps 160 that are attached to a portion of each of the RDL pattern 140.

[0052] Components not described in FIG. 11 are the same as those components explained with reference to FIG. 10. The same reference numerals in FIGS. 10 and 11 denote the same elements that have substantially the same functions and are formed of the same materials and in substantially the same manner. The structure, functions, materials, and effects of the intermediate stud bumps 220, the intermediate RDL pattern 210 and the intermediate insulating layer 230 are substantially the same as those of the stud bump 125, the RDL pattern 140, and the second insulating layer 150, respectively. The

intermediate stud bumps 220 connect the intermediate RDL pattern 210 and the RDL pattern 140. Each intermediate RDL pattern 210 is formed at the bottom of each intermediate stud bump 220. The intermediate insulating layer 230 exposes a portion of the intermediate RDL pattern 210 so it can be connected with the intermediate stud bumps 220.

[0053] In another aspect of the invention, additional intermediate stud bumps, intermediate RDL patterns, and intermediate insulating layers may be formed to make three (or more) layer RDL pattern rather than the two layer RDL pattern illustrated in FIG. 11.

[0054] In the aspects of the invention described above, it is possible to reduce or prevent an inclined portion of a RDL pattern in the art between a solder bump and a chip pad. Such a configuration suppresses cracks in the RDL pattern, even where an underlying insulating layer has a large thickness. Further, a stud bump can be easily and inexpensively formed using a capillary.

[0055] In another aspect of the invention, the wafer level chip scale package is manufactured in the manner depicted in Figures 12-17 so as to not contain a UBM between the chip pad the RDL pattern and to contain a single non-polymeric insulating layer. In this aspect of the invention, and as depicted in Figure 17, the bond pads are first redistributed (as depicted in more detail in Figures 12-15). Then, the stud bumps are formed on the wafer (as depicted in more detail in FIG. 16). The solder balls are then attached to the stud bumps, either directly or by using solder paste, and the solder balls are re-flowed. The resulting packaged semiconductor device can then be mounted on a circuit board as known in the art.

[0056] In this aspect of the invention, and as illustrated in Figures 12-13, a substrate (or chip) 300 (substantially similar to substrate 100) containing IC 305 is obtained. A passivation layer 310 (substantially similar to passivation layer 110) is then formed on substrate 300. A portion of the passivation layer is then removed and a chip pad 315 (substantially similar to chip pad 115) is formed in that exposed portion. The methods used for these processes are substantially similar to those described above.

[0057] Next, as depicted in FIG. 14, a re-distributed (RDL) pattern 340 is formed on directly on the chip pad 315 and the passivation layer 310. The RDL pattern 340 electrically connects the chip pad 315 and the solder bump 365 that is formed during subsequent processing (as described below). The RDL pattern 340 is formed by blanket depositing a metal layer and then removing—typically by masking and etching—the portions of the metal layer not needed for the RDL pattern 340. The RDL pattern 340 can contain any electrically conductive material, such as metals and metal alloys. Examples of such metal and metal alloys include Cu, Al, Cr, NiV, and Ti. In one aspect of the invention, the RDL pattern comprises Al.

[0058] Next, as shown in FIG. 15, an insulating layer 350 is formed to cover the RDL pattern 340. In this aspect of the invention, the material for the insulating layer is blanket deposited on the RDL pattern 340. A masking and etching process is then used to remove a portion of this insulating material in the area of region 375 (where stud bumps 365 will later be formed).

[0059] The material for the insulating layer 350 does not comprise a polymer material like BCB, PI, and EMC. As described above, such materials are often used in conventional WLCSP. To form such layers, however, the structure containing the material is subjected to a high temperature heating process. This heating is necessary to cure the polymer material. Unfortunately, such a high temperature heating process damages the structure underlying the polymeric material including the IC 305 in substrate 300.

[0060] In this aspect of the invention, the insulating layer 350 is not made of polymeric materials. Rather, the insulating layer 350 is made of dielectric non-polymeric materials. Examples of such non-polymeric dielectric materials include silicon nitride, silicon oxide, and silicon oxynitride. Such materials can be deposited by any known method in the art.

[0061] In this aspect of the invention, only a single layer is used as the redistribution layer. In the aspect of the invention shown in Figures 4-10, a UBM and a metal layer are used to redistribute the electrical signal from the chip pad 115 to the stud bump 160. By using only a metal layer in this aspect of the invention, the cost of the manufacturing the

UBM can be eliminated. Thus, this aspect of the invention uses only a single conductive layer as the RDL pattern in the WLSCP.

[0062] As depicted in FIG. 16, the stud bumps are then formed on the exposed portion of the RDL pattern 340 (in the area 375). The stud bumps 365A can be formed by electroplating the material for the stud bumps and with a cladding as known in the art. In this aspect of the invention, the material for the study bumps is Cu and the cladding is a Ni/Au alloy.

[0063] Alternatively, the stud bumps 365B can be formed by a wire bonding process. In this aspect of the invention, a coated wire 380 is attached to the RDL pattern 340 using a capillary 385. As shown in FIG. 16, the bottom of the wire 380 is first bonded to the metal of the RDL pattern 340. Then a coining process is performed to press the wire 380 under a predetermined pressure to form a coined stud bump 365B. By using the capillary, the coined stud bump 365B can be formed with a simple structure and with a simple manufacturing process. In one aspect of the invention, the material for the wire comprises Cu and the coating comprises Pd.

[0064] Finally, as shown in FIG.17, the solder balls are then attached to the stud bumps, either directly or by using solder paste, and the solder balls are re-flowed. Both of these processes are performed using conventional processing that is known in the art.

[0065] In yet another aspect of the invention, the wafer level chip scale package is manufactured in the manner depicted in Figures 18-30. Using this process eliminates the steps of dispensing the solder and reflowing the solder bumps, and optionally eliminates the use of a redistribution trace. In this aspect of the invention, an adhesive film or paste is used between the chip and the substrate.

[0066] In this aspect of the invention, and as illustrated in Figures 18-19, a substrate (or chip) 400 (substantially similar to substrate 100) containing IC 405 is provided. A passivation layer 410 (substantially similar to passivation layer 110) is then formed on chip 400. A portion of the passivation layer is then removed and a chip pad 415 (substantially similar to chip pad 115) is formed in that exposed portion. The methods used for these processes are substantially similar to those described above.

[0067] Next, as depicted in FIG. 20, a re-distributed (RDL) pattern 440 is optionally formed on directly on the chip pad 415 and the passivation layer 410. The semiconductor package can be made with or without the RDL pattern 440 depending on whether re-distribution is necessary. When used, the RDL pattern 440 electrically connects the chip pad 415 and the solder bump 465 that is formed during subsequent processing (as described below). The RDL pattern 440 is formed by blanket depositing a metal layer and then removing—typically by masking and etching—the portions of the metal layer not needed for the RDL pattern 440. The RDL pattern 440 can contain any electrically conductive material, such as metals and metal alloys. Examples of such metal and metal alloys include Cu, Al, Cr, NiV, and Ti. In one aspect of the invention, the RDL pattern comprises Al.

[0068] Next, when the RDL pattern 440 is used, an insulating layer 450 is formed to cover the RDL pattern 440 as shown in FIG. 20. In this aspect of the invention, the material for the insulating layer is blanket deposited on the RDL pattern 440. A masking and etching process is then used to remove a portion of this insulating material in the area of region 475 (where stud bump 465 will later be formed).

[0069] The material for the insulating layer 450 does not comprise a polymer material like BCB, PI, and EMC. As described above, such materials are often used in conventional WLCSP. To form such layers, however, the structure containing the material is subjected to a high temperature heating process. This heating is necessary to cure the polymer material. Unfortunately, such a high temperature heating process damages the structure underlying the polymeric material including the IC 405 in substrate 400.

[0070] In this aspect of the invention, the insulating layer 450 is not made of polymeric materials. Rather, the insulating layer 450 is made of dielectric non-polymeric materials. Examples of such non-polymeric dielectric materials include silicon nitride, silicon oxide, and silicon oxynitride.

[0071] Then studs (or stud bumps) 465 are formed on the structures depicted in Figures 19 (without a redistribution layer) and Figure 20 (with a redistribution layer). As

depicted in FIGs. 21 and 22, the studs 465 are respectively formed on the chip pad 415 and the exposed of the RDL pattern 440 (in the area 475). The stud bumps 465 can be formed by electroplating the material for the stud bumps with a cladding as known in the art. In one aspect of the invention, the material for the stud bumps is Cu and the cladding is Pd. Alternatively, the stud bumps 465 can be formed by a wire bonding process as described above.

[0072] Next, as shown in Figures 23 and 24, an adhesive layer 458 containing conductive particles 459 is applied to the structures of Figures 21 and 22. The adhesive layer 458, as described herein, attaches the chip 400 and the substrate 101 while serving as a limited conductor. Any material functioning in this manner can be used as the adhesive layer 458, including an adhesive material with conductive particles therein. In one aspect of the invention, the adhesive layer 458 comprises an ACF (anisotropic conductive film), an ACP (anisotropic conductive paste) or ICP (isotropic conductive paste).

[0073] The adhesive layer 458 can be applied using any known mechanism in the art. For example, when ACP is used as the adhesive, the layer 458 can be applied by stencil printing. As another example, when ACF is used as the adhesive, the layer 458 can be applied by a film attach process.

[0074] The conductive particles 459 can be any known in the art that can be used with the material of the adhesive. Examples of conductive particles that can be used in adhesive layer 458 are illustrated in FIG. 26. Conductive particle 459a comprises a polymer particle with a metal layer surrounded by an insulating layer. Conductive particle 459b comprises a metal particle surrounded by an insulating layer. The insulating layers in the conductive particles are broken—thereby creating a conductive path—when there is contact between the stud bumps and the substrate (as described below).

[0075] Next, substrate 101 with bond pads 201 (also called electrode pads) is provided. The bond pad 201 is that portion through which the substrate 101 is attached to the chip 400 containing studs 465. The bond pads 201 can be provided on the substrate 101 as known in the art. In one aspect of the invention, the bond pads are provided by a conventional deposition and etching process. The substrate 101 can be made of any

suitable material. One example of a suitable material for the substrate is high glass-transition materials like bis-maleimide triazine (BT) epoxy.

[0076] Next, any known flip chip procedure is used to attach the chip 400 and the substrate 101. In one aspect of the invention, chip 400 containing studs 465 is flipped and placed on the substrate 101 containing the adhesive 458. Alternatively, as depicted in Figure 25, the adhesive layer 458 could be placed on the chip 400 and the substrate 101 flipped and placed on the chip 400. In yet another aspect of the invention, the adhesive layer can be formed on both the chip 400 and the substrate 100 before they are attached. When contacting the substrate 101 and the chip 400, the bond pads 201 and the studs 465 should be substantially aligned as known in the art.

[0077] Next, pressure is applied while the adhesive material is pre-cured, thereby preliminarily connecting chip 400 and substrate 101. The pressure in this process need only be enough to keep the chip 400 and substrate 101 together while the adhesive layer 458 is pre-cured. The pressure that is applied generally can range from about 2 to about 3 Kgf/cm<sup>2</sup> generally for about 0.2 to about 5 seconds.

[0078] The adhesive material is then finally cured by any mechanism in the art, which will depend on the material used. Generally, light and/or heat can be applied to cure the adhesive layer 458. In one aspect of the invention, the adhesive is cured by heating for a sufficient time (greater than about 20 seconds) and at a sufficient temperature (in the range of about 180 degrees Celsius) to finish the curing process.

[0079] The adhesive layer 458 contains conductive particles 459 that will become positioned at intervals inside the adhesive layer 458. Thus, as illustrated in Figure 27, when the chip 400 and the substrate 101 are attached, at least one conductive particle becomes located between the stud bumps 465 and the bond pads 201. Because the bulk of the adhesive layer 458 is not a conductive material, the only conduction between the chip 400 and the substrate 101 is through the conductive particles located between the stud bumps 465 and the bond pads 201.

[0080] After the chip and the substrate have been attached to each other, the resulting structure is as depicted in Figure 27. Then, this structure is encapsulated through any

procedure known in the art. In one aspect of the invention, the encapsulation is carried out, as illustrated in Figure 28, by first applying a support film 501 to the backside of the substrate 201. In one aspect of the invention, the support film is a polyimide (PI) film. Next, the molding compound 502 is applied by any known means, e.g., by transfer molding using an epoxy molding compound, by an applied liquid molding compound in a strip form, or by an array molding. After the molding compound is applied, the support film 501 is removed using any known process in the art.

[0081] After the molding process, the non-singulated semiconductor packages may be electrically tested. Parametric testing is performed while the semiconductor packages are in the form of a strip. After electrical testing, the molded molding material in the semiconductor packages may be laser marked. After laser marking, the semiconductor packages in the array of semiconductor package are singulated using any suitable process, such as by sawing and scribing.

[0082] Figures 18-28 depicts the use of chip pad 415 in the WLCSP. In one aspect of the invention, the chip pad 415 can be eliminated. The chip pad is typically used to protect the chip (IC 405) during subsequent processing. Such a function can also be accomplished by the adhesive layer 458. Thus, in this aspect of the invention, the chip pad 415 can be eliminated as depicted in Figures 29-30.

[0083] In this aspect of the invention, the semiconductor packages have the following advantages. First, the semiconductor packages are more reliable. Known semiconductor packages made using by a flip chip method with an ACF were prone to fail for two reasons. First, formation of non-conductive film on either the contact area or on the conductive particles. Second, there was a loss of mechanical contact between the conductive elements due to either loss of adherence or relaxation of the compressive force. In the invention, these failure mechanisms are reduced or eliminated by encapsulation. The encapsulation reduces moisture attacks and oxidation of the conductive particles. The encapsulation also provides compressive residual stress on the ACF and reduces creep at high temperatures/times.

[0084] A second advantage is that the adhesive material (ACF and ACP) does not contain



substantial amounts of lead and are, therefore, more environmentally friendly than solder. A third advantage is that the semiconductor packages of the invention offer higher resolution capability than those currently using solder paste because of the smaller particle size. A fourth advantage is that the semiconductor packages of the invention are cured at much lower temperatures than those required for soldering, thus reducing thermal stress and is better for thermally sensitive components and the substrate. A final advantage is that less process steps are needed as compared to soldering process, e.g., the flux and flux cleaning processes are not needed.

[0085] Having described these aspects of the invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.